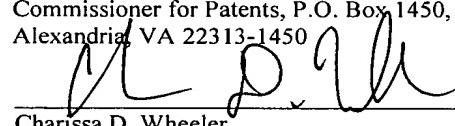


Sole Inventor

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Charissa D. Wheeler

## APPLICATION FOR UNITED STATES LETTERS PATENT

## S P E C I F I C A T I O N

TO ALL WHOM IT MAY CONCERN:

Be it known that I, **Chee Hong Choi**, a citizen of Republic of Korea, residing at 831-1 Dadae 1-dong, Saha-gu, Busan 604-825 KOREA have invented a new and useful **METHOD FOR FABRICATING A METAL-INSULATOR-METAL CAPACITOR IN A SEMICONDUCTOR DEVICE**, of which the following is a specification.

METHOD FOR FABRICATING A METAL-INSULATOR-METAL CAPACITOR  
IN A SEMICONDUCTOR DEVICE

FIELD OF THE DISCLOSURE

[0001] The present disclosure relates generally to semiconductor devices and, more particularly, to a method of fabricating a metal-insulator-metal capacitor in a semiconductor device.

BACKGROUND

[0002] In fabricating highly-integrated memory devices, a capacitor has to provide a relatively high capacitance in a small area. Conventionally, capacitance can be increased by forming a capacitor using a dielectric layer with a large dielectric constant, forming a thin dielectric layer, and/or increasing a cross-sectional area of a capacitor.

[0003] Known multi-layered capacitors or trench-type capacitors have been used to increase a cross-sectional area of a capacitor. A half-spherical polysilicon layer has also been used to that end. However, these known technologies tend to complicate a capacitor structure, reduce process yield, and increase manufacturing cost.

[0004] Dielectric materials including  $\text{SiO}_2/\text{Si}_3\text{N}_4$  are used as commonly used as a dielectric layer of a capacitor. Based on the material used for a capacitor electrode, a polysilicon-insulator-polysilicon (PIP) capacitor structure or a metal-insulator-metal (MIM) capacitor structure may be employed. Thin film capacitors such as PIP capacitors and MIM capacitors are used in analog semiconductor devices requiring precise capacitance values because, in contrast to MOS capacitors and junction capacitors, these capacitors are independent of bias.

[0005] In addition, although the MIM capacitor has a disadvantage because it has smaller capacitance per unit area than that of the PIP capacitor, the former has better VCC (voltage coefficient for capacitance) and TCC (temperature coefficient for capacitance) according to voltage and temperature as compared to the PIP capacitor.

[0006] Figs. 1a through 1f illustrate, in cross-sectional views, the process steps of a known capacitor-fabricating method. Referring to Fig. 1a, a dielectric layer 3 is deposited on a lower metal layer 2 and a substrate 1 with at least a predetermined structure, and an upper metal layer 4 is deposited on the dielectric layer. Referring to Fig. 1b, a MIM capacitor 5 is formed by etching simultaneously the dielectric layer and the upper metal layer using a mask (not shown). Referring to Fig. 1c, an interlayer dielectric 6 is formed on all of the area of the substrate with the MIM capacitor. Referring to Fig. 1d, the interlayer dielectric is etched to form a via hole that connects the upper metal layer and the lower metal layer, respectively, with an uppermost metal layer, and a barrier metal layer 7 is deposited on the via hole. Referring to Fig. 1e, the via hole is filled with a metal plug 8 and flattened to complete the contact via hole. Referring to Fig. 1f, a metal layer is deposited on the metal plug 8 and patterned to form an uppermost metal layer 9, thereby completing a MIM capacitor.

[0007] Korean Patent Publication No. 10-2003-0058317 discloses a MIM capacitor fabricating method that forms an etch stopping layer to prevent the interlayer dielectric from being attacked by etching solution and eliminating an oxide supporting a lower electrode. Another Korean Patent Publication No. 10-2002-0073822 discloses a method of fabricating a MIM capacitor that provides good step coverage and a uniform dielectric layer and forms spacers on lateral walls of a lower electrode.

[0008] However, in these conventional methods the process of forming an MIM capacitor by etching simultaneously an upper metal layer and a dielectric layer, causes a fringing effect at the edge of the MIM capacitor, and is accompanied by bridge, which increases leakage current. The bridge is generated by redeposition of metal etched from the lower metal layer during over-etching necessary for etching a dielectric layer of MIM capacitor. To obviate these problems, the formation of spacers on a lower electrode has been proposed, but such spacers do not completely prevent the bridge due to the difficulty in controlling the process and, in some cases, may significantly complicate processing.

#### BRIEF DESCRIPTION OF THE DRAWINGS

[0009] Figs. 1a through 1f illustrate, in cross-sectional views, known the processing steps.

[0010] Figs. 2a through 2f illustrate, in cross-sectional views, an example method for fabricating an MIM capacitor.

#### DETAILED DESCRIPTION

[0011] As described above, known methods of fabricating an MIM capacitor etch an upper metal layer and a dielectric layer simultaneously using an etch stopping layer formed on a lower metal layer. In addition, these known methods use over-etching to remove the remaining dielectric layer on the lower metal layer. The metal generated by etching of the lower metal layer is redeposited to induce a bridge between the upper and the lower metal layers, which leads to an increase in the leakage current.

[0012] In contrast, the example method described below in connection with Figs. 2a through 2f, uses a sacrificial layer of silicon oxide to protect the lower metal layer despite over-etching.

[0013] An example method for fabricating an MIM capacitor of semiconductor device deposits a metal layer to be used as a lower electrode of the MIM capacitor, deposits a sacrificial layer on the metal layer, removes some area of the sacrificial layer to form an MIM capacitor thereon, deposits a dielectric layer and an upper metal layer, and forms an MIM capacitor by patterning the dielectric layer and the upper metal layer.

[0014] Referring to Fig. 2a, a metal layer to be used as a lower electrode of an MIM capacitor is deposited on a substrate 10 with a predetermined structure. The metal layer is patterned to form a lower metal layer 11. Then, a sacrificial layer 12 is deposited by chemical vapor deposition. The sacrificial layer is used as an etch stopping layer in etching an interlayer dielectric. The sacrificial layer is silicon oxide or silicon nitride and has a thickness of 100~200 Å.

[0015] Referring to Fig. 2b, the sacrificial layer is patterned using a photoresist process, and some area on which an MIM capacitor is formed is removed by dry-etch or wet-etch. Then, an upper metal layer 14 and a dielectric layer 15 are deposited in sequence. The dielectric layer is formed by chemical vapor deposition or atomic layer deposition using a material such as SiN, SiO<sub>2</sub>, Al<sub>2</sub>O<sub>3</sub>, TaON, TiO<sub>2</sub>, Ta<sub>2</sub>O<sub>5</sub>, ZrO<sub>2</sub>, (Ba,Sr)TiO<sub>3</sub> (hereinafter referred to as “BST”), (Pb,Zr)TiO<sub>3</sub> (hereinafter referred to as “PZT”), or (Pb,La)(Zr,Ti)O<sub>3</sub> (hereinafter referred to as “PLZT”). The dielectric layer is a single layer or multi-layer with a thickness of 200~1000 Å.

[0016] Referring to Fig. 2c, an MIM capacitor 16 is formed through patterning and etching the dielectric layer and the lower metal layer and, then, an interlayer dielectric 17 is deposited. The interlayer dielectric may be silicon oxide complex, and is used as an etch stopping layer in etching the dielectric layer and the lower metal layer.

[0017] Referring to Fig. 2d, a via hole 18 is formed. The sacrificial layer on the lower metal layer is etched during the formation of the via hole. Then, as shown in Fig. 2e, the via hole of which a barrier metal layer 19 is deposited on the bottom and the lateral walls is filled with a metal plug 20 and flattened to form a contact via hole. The metal plug is made from a metal selected from the group of tungsten, copper family elements, and platinum family metals. The barrier metal layer is made of a high fusion point metal or nitride thereof, for example, TaN, Ta/TaN, TiN, or Ti/TiN, and is a single layer or multi-layer. The high fusion point metal means a metal having a higher fusion point than that of iron (Fe), 1,535 °C.

[0018] Referring to Fig. 2f, a metal layer is deposited and patterned to form an uppermost metal layer 21 and, finally, the contact is completed.

[0019] In the above-mentioned processes, the metal layers of the MIM capacitor are made of aluminum, a transition element, or an alloy consisting of aluminum and a transition element.

[0020] The above-described example method for fabricating an MIM capacitor can prevent increase in leakage current due to redeposition because a sacrificial layer is used to protect a lower metal layer in spite of over-etching.

[0021] Although certain methods and apparatus have been described herein, the scope of coverage of this patent is not limited thereto. To the contrary, this patent covers all embodiments fairly falling within the scope of the appended claims either literally or under the doctrine of equivalents.